REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of applicants' certified copy of the priority document for the German Patent Application 101 20 054.4, filed April 24, 2001, supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-4 remain in the application. Claim 1 has been amended.

In "Claim Rejections - 35 USC § 102" in items 6 and 7 on pages 2-5 of the above-identified Office Action, claims 1-4 have been rejected as being fully anticipated by U.S. Patent No. 5,483,050 to Fukasawa under 35 U.S.C. § 102(b) and as being fully anticipated by U.S. Patent No. 6,055,500 to Terui et al. under 35 U.S.C. § 102(e).

The rejections have been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the change is found in the original specification and Figs. 3-5 of the instant application.

However, it is initially noted that the object of the

invention of the instant application is to provide for the reduction of the number of contact pads of a semiconductor memory chip. The input and output of digital data according to the prior art requires data transfer by several parallel data buses. Therefore, access is slow. The core concept of the invention of the instant application is to integrate a digital-analog converter and an analog-digital converter directly on the chip. The conversion on the chip makes it possible to use only two pads for row and column addresses instead of several pads provided for the input of digital data. The use of several pads in the prior art has the further disadvantage of rendering the access too slow, because row and column addresses have to be transferred one after another.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a semiconductor component, comprising:

> a semiconductor chip with a semiconductor memory having an array with a plurality of memory cells;
>
> at least one connection contact;
>
> an electrically conductive connection integrated into said semiconductor chip between said at least one connection contact and said semiconductor memory; and

> at least one converter device selected from the group consisting of a digital-analog converter and an analog-digital converter integrated into said semiconductor chip and incorporated in said electrically conductive connection for enabling a utilization of said semiconductor memory with analog signals.

It is thus clear that according to the present invention as claimed, the electrically conductive connection and the at least one D/A or A/D converter are fully integrated into the semiconductor chip. A semiconductor component may include, apart from the semiconductor chip, additional components which are not necessarily integrated into the chip. However, this is an important feature of the invention, which leads to an improvement of the memory chip, that can be used like a standard memory chip except for the fact that the data are input and output in analog format.

This has been emphasized in claim 1 by stating that the electrically conductive connection incorporating the digital-analog converter or the analog-digital converter is part of the chip wiring.

It is believed that the closest prior art remains U.S. Patent No. 5,673,048, which is mentioned in the IDS filed on October 24, 2003 and in the International Search Report.

The Fukasawa reference discloses a magnetic medium processing apparatus having a processing unit 25 shown in Fig. 4. The processing unit 25 is represented in detail in Fig. 5 by an assembly of several different units. As is shown in Fig. 5, a ROM 40 stores programs to be executed by a sub CPU 8 (as described in column 5, lines 25 to 26). A RAM 41 is provided to execute the programs (as described in column 5, line 27). The function of the RAM 41 is explained in more detail in column 6, second paragraph, where the determination of the maximum values of an input signal is described. There is no suggestion in Fukasawa of using the RAM 41 in connection with the analog-digital converter 7 as an integrated semiconductor memory chip. There is no hint either as to how that apparatus might have suggested the concept of substituting standard semiconductor memory chips including digital inputs and outputs with the chip according to the invention of the instant application using analog connections enabled by the monolithic integration of A/D converters.

The Terui et al. reference discloses an information transfer, recording and reproducing device which includes, according to Fig. 1 thereof, a semiconductor memory unit 10 and A/D and D/A converters 6, 13 separate from the semiconductor memory unit 10. Fig. 7 of the reference shows another block diagram of a configuration of an apparatus including a semiconductor memory

103 and a D/A converter 105. The semiconductor memory is specified as being a solid-state memory without any suggestion that two or more of the illustrated components may be monolithically integrated into one semiconductor chip.

It is believed to be clear that the integration of the digital-analog or analog-digital converter into the memory chip according to the invention of the instant application as claimed is neither taught not suggested by the references cited in the above-identified Office Action. It is therefore believed that the rejection of the claims has been overcome.

Clearly, neither Fukasawa nor Terui et al. show an electrically conductive connection integrated into a semiconductor chip and a digital-analog converter or an analog-digital converter integrated into the semiconductor chip and incorporated in the electrically conductive connection, as recited in claim 1 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-4 are solicited.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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September 8, 2004

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